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DESIGN AND IMPLEMENTATION OF AN ON-CHIP PERMUTATION NETWORK FOR MULTIPROCESSOR SYSTEM-ON-CHIP

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ABSTRACT

This paper presents the silicon-proven design of a novel On-chip interconnection networks or Network-on Chips (NoCs) are becoming the de-facto scaling communication techniques in Multi-Processor System-on-Chip (MPSoC) or Chip Multiprocessor (CMP) environment. The proposed network design configured with a 25-bit data width is synthesized and implemented in a 0.13-µm CMOS STD-cell technology. The proposed network employs a pipelined circuit-switching approach combined with a dynamic path-setup scheme under a multistage network topology. The dynamic path-setup scheme enables runtime path arrangement for arbitrary traffic permutations. The circuit-switching approach offers a guarantee of permuted data and its compact overhead enables the benefit of stacking multiple networks. A test chip comprised of 25 testing tiles is designed to test the network. Each testing tile has a 50-bit RISC and FIFO-based test wrappers interfaced with the proposed on-chip network. Tools required Modelsim 6.3 for Debugging and Xilinx 14.3 for Synthesis and Hard Ware Implementation.

KEYWORDS: Guaranteed Throughput, Multistage Interconnection Network, Network-On-Chip, Permutation Network, Pipelined Circuit-Switching, Traffic Permutation